AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A liquid crystal display device comprising: a gate electrode, a gate pad and gate links on a substrate;

first dummy patterns between the gate links;

a gate insulating film on the gate electrode and the gate link;

a semiconductor layer on the gate insulating film;

a source electrode, a drain electrode, a data pad and data links on the semiconductor layer;

a protective film on the source and drain electrodes and the data link; [[and]]

a sealant on the gate links and the data links; and

a pixel electrode on the protective film,

wherein the first dummy patterns have the same vertical structure as any one of the gate links and the data links and are located in the same layer as the gate links and the data links, and

wherein the first dummy patterns are spaced from the gate links by a substantially similar distance to cross entirely the sealant in a direction parallel to the gate links.

2. (Previously Presented) The device of claim 1, wherein the gate links and the first dummy patterns have a same height.

3. (Previously Presented) The device of claim 1, wherein each of the gate links includes the gate electrode, the gate insulation film, the semiconductor layer, and the protective film.

4. (Previously Presented) The device of claim 1, further comprising a sealant on the gate links and the data links.

5. (Currently Amended) The device of claim 1, further comprising second dummy patterns between the data links,

wherein the second dummy patterns are spaced from the data links by a substantially similar distance to cross entirely the sealant in a direction parallel to the data links.

6. (Previously Presented) The device of claim 5, wherein the data links and the second dummy patterns have a same height.

7. (Previously Presented) The device of claim 5, wherein each of the data links includes the source and drain electrodes, the gate insulation film, the semiconductor layer, and the protective film.

8. (Previously Presented) The device of claim 1, wherein the semiconductor layer includes a doped semiconductor layer.

9. (Currently Amended) A method of fabricating a liquid crystal display device, comprising:

forming a gate electrode, a gate pad and gate links on a substrate;

forming first dummy patterns between the gate links;

forming a gate insulating film on the gate electrode and the gate link;

forming a semiconductor layer on the gate insulating film;

forming a source electrode, a drain electrode, a data pad and data links on the semiconductor layer;

forming a protective film on the source and drain electrodes and the data link; [[and]]

forming a sealant on the gate links and the data links; and

forming a pixel electrode on the protective film,

wherein the first dummy patterns are formed into the same vertical structure as any one of the gate links and the data links and simultaneously with any one of the gate links and the data links, and

wherein the first dummy patterns are spaced from the gate links by a substantially similar distance to cross entirely the sealant in a direction parallel to the gate links.

10. (Previously Presented) The method of claim 9, wherein the gate links and the first dummy patterns have a same height.

11. (Previously Presented) The method of claim 9, wherein each of the gate links includes the gate electrode, the gate insulation film, the semiconductor layer, and the protective film.

12. (Previously Presented) The method of claim 9, further comprising the step of forming a sealant on the gate links and the data links.

13. (Currently Amended) The method of claim 9, further comprising the step of forming second dummy patterns between the data links,

the second dummy patterns are spaced from the data links by a substantially similar distance to cross entirely the sealant in a direction parallel to the data links.

14. (Previously Presented) The method of claim 13, wherein the data links and the second dummy patterns have a same height.

15. (Previously Presented) The method of claim 13, wherein each of the data links includes the source and drain electrodes, the gate insulation film, the semiconductor layer, and the protective film.

16. (Previously Presented) The method of claim 9, wherein the semiconductor layer includes a doped semiconductor layer.

17. (Currently Amended) A method of fabricating a liquid crystal display device, comprising:

forming a gate electrode, a gate pad and gate links on a substrate;

forming first dummy patterns between the gate links;

forming a gate insulating film a semiconductor layer on the gate electrode and the gate link;

forming a source electrode, a drain electrode, a data pad and data links on the semiconductor layer;

forming a protective film on the source and drain electrodes and the data link;

patterning the gate insulating film, the semiconductor layer, and the protective film; [[and]]

forming a sealant on the gate links and the data links; and

forming a pixel electrode on the protective film,

wherein the first dummy patterns are formed into the same vertical structure as any one of the gate links and the data links and simultaneously with any one of the gate links and the data links,

wherein the first dummy patterns are spaced from the gate lines by a substantially similar distance to cross entirely the sealant in a direction parallel to the gate links.

18. (Previously Presented) The method of claim 17, wherein the gate links and the first dummy patterns have a same height.

19. (Previously Presented) The method of claim 17, wherein each of the gate links includes the gate electrode, the gate insulation film, the semiconductor layer, and the protective film.

20. (Previously Presented) The method of claim 17, further comprising the step of forming a sealant on the gate links and the data links.

21. (Previously Presented) The method of claim 17, further comprising the step of forming second dummy patterns between the data links,

wherein the first dummy patterns are spaced from the data lines by a substantially similar distance to cross entirely the sealant in a direction parallel to the data links.

22. (Previously Presented) The method of claim 21, wherein the data links and the second dummy patterns have a same height.

23. (Previously Presented) The method of claim 21, wherein each of the data links includes the source and drain electrodes, the gate insulation film, the semiconductor layer, and the protective film.

24. (Previously Presented) The method of claim 17, wherein the semiconductor layer includes a doped semiconductor layer.

25. (Previously Presented) The device of claim 5, wherein the second dummy patterns are formed into the same vertical structure as any one of the gate links and the data links.

26. (Previously Presented) The method of claim 13, wherein the second dummy patterns are formed into the same vertical structure as any one of the gate links and the data links.

27. (Previously Presented) The method of claim 21, wherein the second dummy patterns are formed into the same vertical structure as any one of the gate links and the data links.